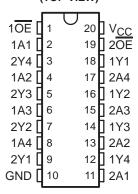
SCAS790B - DECEMBER 2004 - REVISED JANUARY 2008

- Qualified for Automotive Applications
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Specified From -40°C to 85°C and -40°C to 125°C
- Max t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DW OR PW PACKAGE (TOP VIEW)



description/ordering information

This octal buffer/line driver is operational at 1.5-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION†

TA	PACKAGE	‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
4000 1- 40500	SOIC - DW	Reel of 2000	SN74LVC244AQDWRQ1	LVC244AQ
-40°C to 125°C	TSSOP – PW	Reel of 2000	SN74LVC244AQPWRQ1	LVC244AQ

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

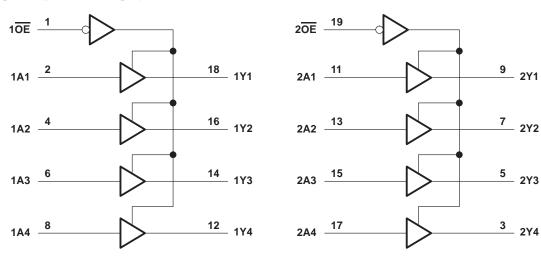


[‡]Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DW package	58°C/W
PW package	83°C/W
Storage temperature range, T _{stq}	–65°C to 150°C
Power dissipation, P_{tot} ($T_A = -40^{\circ}$ C to 125°C) (see Notes 4 and 5)	500 mW

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The value of V_{CC} is provided in the recommended operating conditions table.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 - 4. For the DW package, above 70°C the value of P_{tot} derates linearly with 8 mW/K.
 - 5. For the PW package, above 60°C the value of Ptot derates linearly with 5.5 mW/K.



recommended operating conditions (see Note 6)

			T _A =	T _A = 25°C		-40 TO 85°C		-40 TO 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V	
VCC	Supply voltage	Data retention only	1.5		1.5		1.5		V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$			
VIH	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		V	
	voltage	V _{CC} = 2.7 V to 3.6 V	2		2		2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		0.35 × V _{CC}		$0.35 \times V_{CC}$		
VIL	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7		0.7		0.7	V	
	voltage	V _{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8		
VI	Input voltage		0	5.5	0	5.5	0	5.5	V	
Vo	Output voltage		0	VCC	0	VCC	0	VCC	V	
		V _{CC} = 1.65 V		-4		-4		-4		
١.	High-level	V _{CC} = 2.3 V		-8		-8		-8	4	
ЮН	output current	V _{CC} = 2.7 V		-12		-12		-12	mA	
		V _{CC} = 3 V		-24		-24		-24		
		V _{CC} = 1.65 V		4		4		4		
۱.	IOL Low-level output current	V _{CC} = 2.3 V		8		8		8	4	
IOL		V _{CC} = 2.7 V		12		12		12	mA	
		VCC = 3 V		24		24		24		

NOTE 6: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		.,	T _A =	25°C		-40 TO 8	5°C	-40 TO 12	25°C	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V _{CC} - 0.2		V _C C - 0.3		
	I _{OH} = -4 mA	1.65 V	1.29			1.2		1.05		
V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			1.7		1.55		V
VOH	1 40 m A	2.7 V	2.2			2.2		2.05		V
	I _{OH} = -12 mA	3 V	2.4			2.4		2.25		
	$I_{OH} = -24 \text{ mA}$	3 V	2.3			2.2		2		
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.1		0.2		0.3	
	$I_{OL} = 4 \text{ mA}$				0.24		0.45		0.6	
VOL	I _{OL} = 8 mA	2.3 V			0.3		0.7		0.75	V
	I _{OL} = 12 mA	2.7 V			0.4		0.4		0.6	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55		0.55		0.8	
lį	V _I = 5.5 V or GND	3.6 V			±1		±5		±20	μΑ
l _{off}	V_I or $V_O = 5.5 V$	0			±1		±10		±20	μΑ
loz	V _O = 0 to 5.5 V	3.6 V			±1		±10		±20	μΑ
	V _I = V _{CC} or GND	261/			1		10		40	
Icc	$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{\dagger} \qquad \text{IO} = 0$	3.6 V	1			10		40	μΑ	
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500		500		5000	μΑ
Ci	V _I = V _{CC} or GND	3.3 V		4						pF
Co	$V_O = V_{CC}$ or GND	3.3 V		5.5						pF

[†] This applies in the disabled state only.



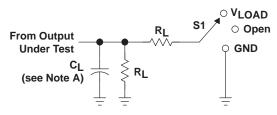
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	.,	T	չ = 25°C	;	-40 TO	85°C	-40 TO	125°C		
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			1.5 V		7	14.4		14.9		16.4		
		·	1.8 V ± 0.15 V		5.9	10.4		10.9		12.4		
t _{pd}	Α	Υ	2.5 V ± 0.2 V		4.2	7.4		7.9		10	ns	
			2.7 V		4.2	6.7		6.9		8.2		
			3.3 V ± 0.3 V		3.9	5.7		5.9		7.2		
			1.5 V		8.3	17.8		18.3		19.8		
		Y	1.8 V ± 0.15 V		6.4	12.1		12.6		14.1	ns	
^t en	ŌĒ		2.5 V ± 0.2 V		4.6	9.1		9.6		11.7		
				2.7 V		5	8.4		8.6		10.3	
		·	3.3 V ± 0.3 V		4.5	7.4		7.6		9.4		
			1.5 V		7.2	15.6		16.1		17.6		
			1.8 V ± 0.15 V		5.8	11.6		12.1		13.6		
^t dis	ŌĒ	Υ	2.5 V ± 0.2 V		3.7	7.3		7.8		9.9	ns	
		2.7 V		3.8	6.6		6.8		8.6			
			3.3 V ± 0.3 V		3.8	6.3		6.5		8		
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns	

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	VCC	TYP	UNIT	
				1.8 V	43	
		Outputs enabled	f = 10 MHz	2.5 V	43	
	Device discipation consists and how how the second			3.3 V	44	
C _{pd}	Power dissipation capacitance per buffer/driver		f = 10 MHz	1.8 V	1	pF
		Outputs disabled		2.5 V	1	
				3.3 V	2	

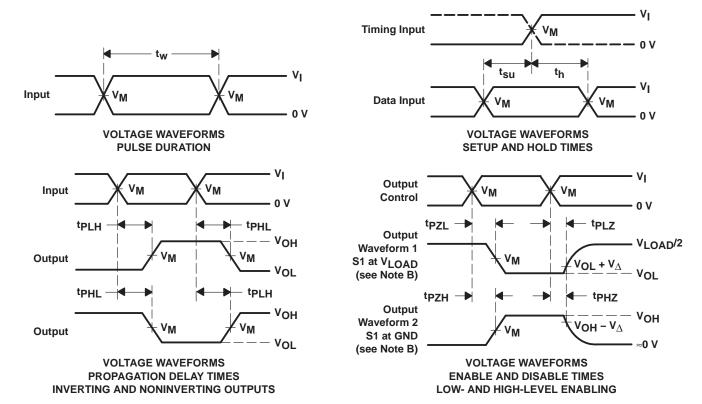
PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

LOAD CIRCUIT

	INF	PUTS	.,			_	.,
VCC	٧ı	t _r /t _f	νM	VLOAD	CL	RL	$v_{\scriptscriptstyle\Delta}$
1.5 V	VCC	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	VCC	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	VCC	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzI and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







i.com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CLVC244AQDWRG4Q1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CLVC244AQPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC244AQDWRQ1	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR Level-1-235C-UNLIM
SN74LVC244AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC244A-Q1:

Catalog: SN74LVC244A

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



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